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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/541,857	04/03/2000	James Digby Collier	491.039US1	4161

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EXAMINER	
LAM, TUAN THIEU	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/541,857	Applicant(s) COLLIER ET AL.	
	Examiner Tuan T. Lam	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *59-84* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *59-84* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This is a response to the amendment filed 4/14/2003. Claims 59-84 are pending.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 59-70, 72-82 and 84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kouno (JP 60-224319), newly cited prior art in view of Schilling et al. (Electronic circuits, 1989, pages 138-151). Figure 9 of Kouno shows a frequency divider circuit comprising a first signal means (not shown) for generating a first periodic signal (CL1) to be frequency divided by the frequency divider, said frequency divider comprises an input terminal for receiving the first periodic signal, an even number of amplifier stages (two amplifier stages 6-8; 9-11) connected in series, with an output of a last amplifier stage (9-11) connected to input of a first amplifier stage (6-8) and each amplifier each having an associated propagation delay and a transistor (7-8; 9-11) coupled between a supply terminal Vdd and a reference terminal (VSS) for modulating delay through the associated amplifier, the first periodic signal (CL1) applied to the first input terminal to a control electrode of the transistor of the odd amplifier stage (6-8), and for applying the second clock signal (CL2) to a control electrode of said transistor of the even amplifier (9-11) to modulate the propagation delays through the associated amplifier stages about half the period of said first and second periodic signals so that when the propagation delay through the even

amplifier stage (9-11) decreases, the propagation delay through the odd amplifier stage increases, and an output terminal (Q, Q/) for outputting a generated frequency divided signal.

The difference seen between Kouno reference and the present invention is that Kouno does not specify the first and second periodic signals as analogue periodic signals having an amplitude which causes said transistors to be not fully open or fully closed but to act as variable resistance as called for in claims 59, 75 and 84. Schilling et al. teaches that field effect transistor is a voltage controlled device. The field effect transistor can operate as a variable resistance given a proper input signal. When the field effect transistor operated in this region, the field effect transistor is not fully open or fully closed. Therefore, it would have been obvious to a person skilled in the art at the time of the invention was made to recognize that the Kouno's frequency divider will work equally well with analog clock signals, since the field effect transistors possesses properties that is adaptable to different shape of input signals as taught by Schilling et al. Therefore, outside of non-obvious results, the obvious of using analog signals as input signals instead of square wave to vary the resistance of field effect transistors in a frequency divider will not be patentable under 35USC 103(a).

3. Regarding claim 60, the number of amplifiers is two.

4. Regarding claim 61, Kouno shows a single frequency divider. However, it is known and obvious to one skilled in the art to cascade a plurality of Suzuki et al.'s frequency divider to obtain a desired frequency divided signal. Therefore, the limitation of cascading a plurality of frequency dividers will not be patentable under 35USC 103(a).

5. Regarding claims 62 and 76, each amplifier stage 6-8; 9-11 comprises differential amplifier.

6. Regarding claim 63, logic circuitry includes said transistor in each amplifier stage is seen as transistors in boxes 7, 8 and 10, 11.

7. Regarding claims 64, 77 and 79, each amplifier stage of Kouno inherently has hysteresis characteristics which varies in response to the clock signals.

8. Regarding claim 78, the limitations recited therein is inherently present in Kouno.

9. Regarding claims 65-67 and 80-81 each amplifier stage is CMOS.

10. Regarding claims 68 and 69, said first transistors are seen as transistors in boxes 7-8 for the odd stage 6-8, and for the even stage 242, said second transistors are seen as the transistors in boxes 10, 11. Said first and second transistors are coupled in series between the supply terminal and the reference terminal.

11. Regarding claims 70 and 82, Kouno does not specifically indicate the periodic signal (CLOCK) in a range of 100 Mhz. However, it is known that CMOS technology is capable of operating with frequencies of 100 Mhz or higher. Therefore, the limitation of using the clock signal at 100 Mhz is seen to be inherently presently in Kouno's frequency divider.

12. Regarding claim 72, first and second inverters are seen as transistors 6 and 9.

13. Regarding claim 73, N channel transistors are seen as transistors in boxes 7, 8, 10, 11.

14. Regarding claim 74, Kouno does not disclose the size of n channel controlling transistors (7, 8) is larger than the size of n channel transistors (the n channel transistors of the inverters in boxes 6). However, it is notoriously well known to implement the n channel controlling transistors with a larger size in order to reset the crossed inverters (6; 9) at a quicker speed thus preventing an erroneous operation. Therefore, the limitation of having n channel controlling

transistor at a larger size than the size of the n channel inverting transistors will not be patentable under 35USC 103(a).

15. Claims 71 and 83 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kouno (JP 60-224319), newly cited prior art, in view of Schilling et al. (Electronic circuits, 1989, pages 138-151) and in further view of Maemura (USP 5,172,400). The combination of Kouno and Schilling et al. teaches recited in claims 59 and 75, as noted above, but fails to show logic circuitry connected in series between at least two of the amplifier stages in order to enable division by ratios other than simple powers of two as called for in claims 71 and 83. Figure 15 of Maemura reference teaches the use of a logic circuitry (41) implemented in between two amplifier stage to obtain a division ratio other than power of two. Therefore, it would have been obvious to a person skilled in the art at the time of the invention was made to include the logic circuitry (41) of Maemura in the circuit arrangement of Kouno's figure for the flexibility of obtaining a frequency divided output other than power of two.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 703-305-3791. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P CALLAHAN can be reached on 730-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Tuan T. Lam
Primary Examiner
Art Unit 2816

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May 10, 2003